

No. SRITW/Prin/2019 Date: 21-09-2019

#### **CIRCULAR**

All the students are hereby informed that our college is offering value-added courses. Interested students can register their names with the respective course coordinator. A detailed brochure regarding the courses is available in the notice board.

**Criteria for Certification**: Attendance >=75% and marks secured >=70%.

\*: Imp dates:\*

Registrations opening date: 24-09-2019

Registrations closing date: 01-10-2019

**Course start date: 19-10-2019** 

Course end date: 22-11-2019

Courses offered:

- 1. Computer fundamentals
- 2. Embedded Systems
- 3. Raspberry PI & other Peripheral Systems
- 4. Migration Techniques in Cloud Computing

Principal

**Principal** 

Sumathi Reddy Institute of Technology for Women Ananthasagar (V), Hasanparthy (M)

WARANGAL - 506 371 (TS)

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HOD (CSE, ECE, EEE, H&SC)

Administrative Officer

In-charge, Exam Branch

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Notice Board

To be read in classrooms



#### A Course on

#### **EMBEDDED SYSTEMS**

Organized by the Department of Electronics and Communication Engineering

#### Course Objectives:

- To introduce the Building Blocks of Embedded System.
- To Introduce Bus Communication in processors, Input/output interfacing.
- To impart knowledge in various processor scheduling algorithms.
- To introduce Basics of Real time operating system and example tutorials to discuss on one real time operating system tool.
- To understand embedded-system programming and apply that knowledge to design and develop embedded solutions.
- The course will introduce various interfacing techniques for popular input devices including sensors, output devices and communication protocols

#### **Course Co-ordinator:**

Mr.Ch.Siddhardha Asst. Prof. CSE Dept



Venue:

Lecture Hall1: 117 Lecture Hall2: 118 For registration contact: 9885378822

Course start date: 19-10-2019 Course end date: 22-11-2019

#### Course Instructors:

1.Mr. A.Mahesh Asst. Prof, CSE 2. Mr.D. Koteshwar Rao Asst. Prof, ECE

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Ananthasagar (V), Hasanparthy (M)

Timings: 3x1012MGALOCOM71 (TS)

### **EMBEDDED SYSTEMS Date: 19-10-2019 to 22-11-2019**

#### **Course Content**

- Introduction to Embedded Systems and Computer Systems Terminology, Modular approach
- to Embedded System Design using Six-Box model: Input devices, output devices,
- embedded computer, communication block, host and storage elements and power supply.
- Microcontroller Based Embedded System Design, salient Features of Modern, Microcontrollers, elements of Microcontroller Ecosystem and their significance.
- Design of Power Supply for Embedded Systems, Linear Regulator Topologies, switching Power Supply Topologies. Power Supply Design Considerations for
- Embedded Systems.
- Introduction to MSP430 Microcontroller: MSP430 CPU Architecture, Programming Methods for MSP430, Introduction to Lunchbox Platform.
- **Fundamentals of Physical Interfacing**: Connecting Input Devices, switches, Keyboard and Output devices, LEDs, Seven Segment Displays (SSD)Advanced Physical Interfacing Driving load high side, low side and H-bridge, multiplexing displays including Shaft encoder.
- Programming the MSP430, Basics of version control system Git, Installing and using Code Composer Studio (CCS), Introduction to Embedded Interfacing LEDs and Switches with MSP430 using Digital Input and Output.
- MSP430 Clock and Reset System, MSP430Clock sources and distribution, Types of Reset sources. Handling Interrupts in MSP430, Writing efficient Interrupt Service Routine (ISR).
- Interfacing Seven Segment Displays and Liquid Crystal Displays with MSP430.
   Low Power Modes in MSP430, Introduction to MSP430 Timer Module and its Modes of Operation.
- Generating Pulse Width Modulation (PWM) using Timer Capture Mode, DC operation in MSP430, Interfacing analog inputs. Generating random numbers using LFSR and other methods. Adding DAC to MSP430, custom Waveform generation using MSP430.
- Timer Capture Modes, Measuring frequency and time period of external signals and events.
- **Serial Communication Protocols:** UART, SPI, I2C, Interfacing Universal Serial Communication Interface (USCI) Module of the MSP430 for UART Communication, Advanced Coding Exercises based on Interrupt driven Programming, Building an Electronics Project.
- Circuit Prototyping techniques, Designing Single Purpose Computers using Finite State Machine with Data path (FSMD) approach, MSP430 Based Project Design and Implementation. Recap of Course Coverage.

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Phone no: 0870-2818302. Email: principal@sritw.org.



- **Interfacing of Motors:** Introduction to Motors, Types of Motors used in Embedded System, Programming & Controlling of motors in Embedded Systems, Timers & Counters Programming, Introduction to Timers & Counters, Difference between Timer and Counter, Description of SFR associated with Timers & Counters, Programming of Timers & Counters Serial Communication Programming, Introduction to Serial Communication,
- Types of Serial Communication, Description of SFR associated with Serial Communication
- Programming of UART, Interfacing Of ADC
- Introduction to ADC, Programming of ADC
- Sensor Interfacing: Introduction to sensing devices, Interfacing of IR Sensors, Interfacing of Temperature Sensor.
- Embedded Networking:I2C Bus Standard, Bluetooth, Zigbee, USB,UAR
- Linux Fundamentals & Device Driver Programming: Linux Fundamentals, Linux Command, Editors.
- Introduction to Device Driver: The Role of Device Driver, Kernel Module Vs. Application, Types of Device Driver, Character Driver, Block Driver & Network Driver

#### **Course Outcomes**

After completion of the course students will be able to learn

- About the embedded system design using a building block approach, which allows one to visualize the requirement of an embedded system and then to design it efficiently.
- The course will teach embedded system design using a microcontroller, namely Texas Instruments MSP430 low power microcontroller.
- The course will introduce various interfacing techniques for popular input devices including sensors, output devices and communication protocols.
- It will teach power supply design for embedded applications. It will also teach effective embedded programming techniques in C and how to maintain code using GIT.

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## SUMATHI REDDY INSTITUTE OF TECHNOLOGY FOR WOMEN

Affiliated to JNTUH - Approved by AICTE

#### List of students Registered for Embedded Systems

Dist of students	registered for Embedded Systems
Batch: 1	Date: 19-10-2019 to 22-11-2019

Batch: 1		Date: 19-10-2019 to 22-11-2019
S. no	Roll no	Name of the Student
1	166Y1A0476	VEMULA SACHIVYA REDDY
2	166Y1A0477	VENUVANKA MANSI
3	166Y1A0478	VURLUGONDA SOUMYA
4	166Y1A0479	ZILPELLIWAR SREEJA
5	16C31A04D3	SUNKISHALA RACHANA
6	176Y5A0401	ALAKANTI SHUSHMA
7	176Y5A0402	ALUGOJU SPANDANA
8	176Y5A0403	EJJAGIRI ANUSHA
9	176Y5A0404	GORAD ASHWINI
10	176Y5A0405	MANTHRI SHASHIKALA
11	176Y5A0406	MODEM DIVYA
12	176Y5A0407	PABBU ANUSHA
13	176Y5A0408	SAMALA VYSHALI
14	176Y5A0409	SOORA SAI LAXMI
15	186Y5A0401	ADEPU DEEKSHA
16	186Y5A0402	ADEPU DEVIKA
17	186Y5A0404	CHALLA AKHILA
18	186Y5A0405	GANDRA SOUMYA
19	186Y5A0406	GUDIKANDULA PREETHI
20	186Y5A0407	JANGAM RASHMA
21	186Y5A0408	KADARI NETHRA
22	186Y5A0409	KATKURI DEEPIKA
23	186Y5A0410	KONDABOINA VENNELA
24	186Y5A0411	KOTHA PRANAYA
25	186Y5A0412	KOTHAKONDA PRIYADARSHINI
26	186Y5A0413	PINNINTI HIMABINDU
27	186Y5A0414	PONNAM GOUTHAMI
28	186Y5A0415	RANGU PRIYANKA
29	186Y1A05B2	TULA AKANKSHA
30	186Y1A05B3	UDUTHA DIVYA
31	186Y1A05B4	UTNOORI NITHYA SRI
32	186Y1A05B5	VEDA SRESHTA MADAVA PEDDI
33	186Y1A05B6	VENGALA VYSHNAVI

ch Siddhu Course-coordinator

Principal

Sumathi Reddy Institute of Technology for Women

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## SUMATHI REDDY INSTITUTE OF TECHNOLOGY FOR WOMEN

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Batch: 2

Date: 19-10-2019 to 22-11-2019

2	Date.	19-10-2019 to 22-11-2019
S. no	Roll No	Name of the Student
1	186Y1A05B7	VIJAYAGIRI SAI NIKITHA
2	196Y5A0501	ALIYA MEHREEN
3	196Y5A0502	AYESHA SULTHANA
4	196Y5A0503	BALASANI VENNELA
5	196Y5A0504	BODDUNA CHANDANA
6	196Y5A0505	CHINDAM AKANKSHA
7	196Y5A0506	MUSUKU PRAVALIKA
8	196Y1A05B6	VENNAMANENI DEEPIKA
9	196Y1A05B7	YADA SRIVALLI
10	196Y1A05B8	YERRABELLI SRINITHYA
11	196Y1A05B9	POGULA INDU
12	206Y5A0501	AKULA CHANDANA
13	206Y5A0502	KOTA SAI KASTURI
14	206Y5A0503	LAKKA PRIYA
15	206Y5A0504	MANDA SAI ANJANI
16	206Y5A0505	MOHAMMAD SHABANA ANJUM
17	206Y5A0506	PALIKA DIVYA DARSHINI
18	206Y5A0507	PANGA PAVANI
19	206Y5A0508	PASUNURI ESTHERA
20	206Y5A0509	SIRIMALL TRIVENI
21	206Y5A0510	VEMURI AKSHITHA
22	206Y1A0412	BOPPA AKHILA
23	206Y1A0413	BUDDHE SANGEETHA
24	206Y1A0414	BURLA HARIKA
25	206Y1A0415	CHERUKUPALLY KEERTHANA
26	206Y1A0416	CHINTHAREDDY DIVYASRI
27	206Y1A0417	DEVATHI MADHUMITHA
28	206Y1A0418	EMMADI SATHWIKA
29	206Y1A0419	ENUGALA SOUJANYA
30	206Y1A0420	GORANTALA HARSHITHA
31	206Y1A0421	GOURI PRIYA YAMSANI
32	206Y1A0422	GUMMADAVELLI DEEKSHITHA
33	206Y1A0423	HATKAR DEEPIKA
34	206Y1A0424	HUZAIFA GAZNAM
35	206Y1A0425	JAKKULA VAISHNAVI
36	206Y1A0426	JANAGANI BHAVANA
37	206Y1A0427	JANGALA LAXMI PAVANI
		JERIPOTHULA CHANDANA
38	206Y1A0428 206Y1A0429	KADIVENDI POOJITHA
39		KALERU SAI SRUTHI
40	206Y1A0430	KOTHAKONDA HARIKA
41	206Y1A0431	KUCHANA AMULYA
42	206Y1A0432	MADASU MADHU SREE
43	206Y1A0433	MANDA AISHWARYA
44	206Y1A0434	MANDA KEERTHANA
45	206Y1A0435	1
46	206Y1A0723	YARA SAISRI

Course-coordinator

Principal

Sumathi Reddy Institute of Technology for Women

Ananthasagar (V), Hasanparthy (M)

Ananthasagar, Hasanparthy, Warangal -506371, Telangana. Website: WARVANGAPTS 506 371 (TS) Phone no: 0870-2818302. Email: principal@sritw.org.

EMBEDDED SYSTEMS

BATCH-1

Academic year 2019-20 Course Instructor: A.MAHESH

		DATE:	19/10	layio	21/10	20/1	22/10	23/10	24/10	25/10	26/10	29/0	20/10	30/0	30/10	31/10	1/0	7/11	3/4	4/11	4	5/4	5/11	6/1	7/0	7/11	8(11	11/11	13/,,	13/01	uh	4/1
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1	166Y1A0476	VEMULA SACHIVYA REDDY	1	2	A	3	4	5	6	7	8	A	9	10	11	12	13	lu	15	16	17	18	A	19	20	21	22	22	24	25 2	26 2	7
2	166Y1A0477	VENUVANKA MANSI	1	2	3	u	5	A	6	7	8	9	10	11	12	A	13	lu	15	16	17	18	19	20	21	22	A	7.3	24	Lance III		1
3	166Y1A0478	VURLUGONDA SOUMYA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		20	21	22	23	24	25	- 26	27		1000	30
4	166Y1A0479	ZILPELLIWAR SREEJA	1	2	3	u	A	5	6	7	8	A	9	10	11	12	13	iu	15	A	16	17	18	19	20	21	22	23			26	27
5	16C31A04D3	SUNKISHALA RACHANA	1	2	3	u	5	6	7	8	9	10	11	12	13	ly	15	16	17	18	19	20	21	22	23	24	25	26	-			30
6	176Y5A0401	ALAKANTI SHUSHMA	1	2	3	4	5	6	7	8	9	10	11	12_	A	13	14	A	15	16	17	18	19	20	A	20	22	100	24		26	2.7
7	176Y5A0402	ALUGOJU SPANDANA	1	2	A	3	u	5	6	A	7	8	9	10	"	12	13	lu	15	16	A	17	18	19	20	20	21	- A-191	24		28 2	7
8	176Y5A0403	EJJAGIRI ANUSHA	1	2	3	u	5	6	7	8	9		11	12	13	14	15	16	17	18	19	20	A	21	22	23	24	25	26			29
9	176Y5A0404	GORAD ASHWINI	1	2	3	u	5	6	7	8	9	A	0	II	12	13	14	15	16	17	18	19		91	22	23	24	25	24	23 2	8 2	9
10	176Y5A0405	MANTHRI SHASHIKALA	1	2	3	ч	9	6	7	8	9	to	11	12	13	tu	15	A	16	17	18	19	20	21	22	23	24	25	26	272	0	201
11	176Y5A0406	MODEM DIVYA	1	2	3	u	5	6	7	8	9	10	11	12	13	lu	15	16	17	18	19	20	A	21	22	23	24	20	26	272	8 7	á
12	176Y5A0407	PABBU ANUSHA	1	2	3	A	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	22	24	A	25	1	2 1	2
13	176Y5A0408	SAMALA VYSHALI	1	2	3	u	A	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	28	26	27	-	29
14	176Y5A0409	SOORA SAI LAXMI	1	2	2	u	5	6	7	8	9	10	11	12	13	14	11	16	17	18	200	20	21	22	22	24	25	26			-	30
15	186Y5A0401	ADEPU DEEKSHA	1	2	3	u	7	6	A	4	8	9	10	11	A	12	13	14	19	16	17	A	18	19	20	21	22	23	24	A		26
16	186Y5A0402	ADEPU DEVIKA	1	2	3	ч	4	6	F	8	9	10	11	12	13	14	18	16	+	18	19	20	21	22	23	nei	25	28	27	NODE I	-	30
17	206Y1A0432	KUCHANA AMULYA	1	A	2	3	4	5	6	7	8	9	10	12	12	13	14	15	16	17	18	9	20	21	22	23	24	25	26		Transit Inc	29
18	186Y5A0404	CHALLA AKHILA	1	2	2	u	5	6	7	8	9	A	10	11	12	13	14	15	16	19	18	q	20	21	22	23	24	25	2G		Variation 1	C
19	186Y5A0405	GANDRA SOUMYA	A	1	2	3	u	5	6	7	8	9	10	11	12	13	4	14	15	16	17	18	19	20	21	A	22	23	24	25- 2	26, 3	17
20	186Y5A0406	GUDIKANDULA PREETHI	1	2	3	u	5	6	7	8	9	10	U	12	13	14	15	16	17	18	19	20	21	22	23	24	24	28	27	28 2	9:	30
21	186Y5A0407	JANGAM RASHMA	A	1 3	5	3	u	5	A	6	1	8	9	10	11	12	13	A	A	lu	15	-16	17	18	19	20	21	22	25			26
22	186Y5A0408	KADARI NETHRA	1	2	3	u	5	6	7	8	9	10	()	12	3	14	15	16	17	18	19	20	21	22	22	24	35	re	29	28 2	9 3	30
23	186Y5A0409	KATKURI DEEPIKA	1	2	3	u	4	6	7	A	8	a	10	A	U	12	13	14	15	16	17	18	19	20	21	22	23	24	25		-	8
24	186Y5A0410	KONDABOINA VENNELA	t	2	3	4	25	6	7	5	9	10	u	12	13	14	15	A	16	17	18	19	20	21	22	23	24	A	25	26 2	_	8
25	186Y5A0411	KOTHA PRANAYA	1	2	A	3	4	5	6	7	8	9	10	11	12	13	14	15	(6	17	18	19	20	21	22	23'	24	25	16			9
26	186Y5A0412	KOTHAKONDA PRIYADARSHINI	1	2	3	u	5	A	6	7	8	9	10	U	12	13	3	15	16	17	18	19	20	21	22	200	24	25	200		8 4	4
27	186Y5A0413	PINNINTI HIMABINDU	1	2	3	u	5	6	7	8	9	10	11	12	13	lu	15	16	12	1%		20	21 7	12	23	2	2	Les	LA	-	9 0	10
28	186Y5A0414	PONNAM GOUTHAMI	1	2	3	A	ú	5	6	7	8	9	10	U	12	12	Iu	15	A	16	A	18	19	20	21	20	22	24	25	28-	22	4
29	186Y5A0415	RANGU PRIYANKA	+	2	3	u	5	6	A	A	8	9	10	11	12	(3	14	15	16	17	18	A	19	20	21	22	Ti	P	EX.	160	4-	18
30	186Y1A05B2	TULA AKANKSHA	1	2	3	u	5	6	7	8	9	10	11	192	12	iu	18	66	12	18	19	Su	Mati	1,70	day	75 lit	TO O	166	mair	gy for	WOR	gen
31	186Y1A05B3	UDUTHA DIVYA	A	*	2	3	ú	5	6	7	8	9	(0)	A	11	12	13	lu	15	16	17	18	Ana	onth	asa	gar	99	Has	anc	anthy	(M)	1
32	186Y1A05B4	UTNOORI NITHYA SRI	1	12	2	u	5	6	7	8	9	to	VI	12	12	lu	15	16	17	18	19	20	21	WA	RA	VG/	de	506	271	1331	91:	30
33	186Y1A05B5	VEDA SRESHTA MADAVA PEDDI	1	12	3	u	5	6	7	8	9	A	10	11	12	13	lu	15	16	14	18	19	20	21	22	23	24	25	A	262	7 2	8

Academic year 2019-20

Course Instructor: A.MAHESH BATCH-1 EMBEDDED SYSTEMS DATE: NAME SNO ROLL NO 166Y1A0476 VEMULA SACHIVYA REDDY 166Y1A0477 VENUVANKA MANSI 32 33 34 VURLUGONDA SOUMYA 166Y1A0478 A ZILPELLIWAR SREEJA 166Y1A0479 16C31A04D3 SUNKISHALA RACHANA A 176Y5A0401 ALAKANTI SHUSHMA ALUGOJU SPANDANA 176Y5A0402 A 33 176Y5A0403 EJJAGIRI ANUSHA 33 34 176Y5A0404 GORAD ASHWINI A 31 32 MANTHRI SHASHIKALA 176Y5A0405 MODEM DIVYA A 176Y5A0406 1. 176Y5A0407 PABBU ANUSHA SAMALA VYSHALI 176Y5A0408 100% 176Y5A0409 SOORA SAI LAXMI A 186Y5A0401 ADEPU DEEKSHA 33 34 ADEPU DEVIKA 186Y5A0402 KUCHANA AMULYA 206Y1A0432 186Y5A0404 CHALLA AKHILA 186Y5A0405 GANDRA SOUMYA 32 A GUDIKANDULA PREETHI 186Y5A0406 88% 291 30 JANGAM RASHMA 186Y5A0407 186Y5A0408 KADARI NETHRA 186Y5A0409 KATKURI DEEPIKA 941/ 186Y5A0410 KONDABOINA VENNELA 186Y5A0411 KOTHA PRANAYA 186Y5A0412 KOTHAKONDA PRIYADARSHINI A PINNINTI HIMABINDU 186Y5A0413 186Y5A0414 PONNAM GOUTHAMI 186Y5A0415 RANGU PRIYANKA Sulnathi Reddy Institute of Technology for Women 100 % 186Y1A05B2 TULA AKANKSHA Ananthasagar (V), Hasanparthy (M) 30/31 UDUTHA DIVYA 186Y1A05B3 WARANGAL - 506 371 (TS) 32 34 UTNOORI NITHYA SRI 186Y1A05B4 29 30 31 VEDA SRESHTA MADAVA PEDDI 186Y1A05B5

Course Co-odinator

	D	ATE:	19/	19/	171	20/	12/1-	23	24/	15/1-	36/	7	4/]	34,	39	31/	7,	2/1	2/11	W.	el.	51.	51.	6/	41	71.	8/	111/	13	1/12/	tut	1
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1	186Y1A05B7	VIJAYAGIRI SAI NIKITHA	1	2	3	u	A	5	6	1000	8	-		0	1	2	13	14	ıs	1/	17-	19		20	21	A	20	2 23				-
2	196Y5A0501	ALIYA MEHREEN	1	A	2	3	ч	5	6		7	0		10	11	A	12	13	IU	15	16	12	-	19	20		22	23		_		and the same
3	196Y5A0502	AYESHA SULTHANA	1	2	3	u	5	6	7	8	9			12	13	14	15	16	17	18	19	20	21	22		110000	25	1	27			_
4	196Y5A0503	BALASANI VENNELA	1	2	3	q	5	6	7	2	a		10	11	12	12	iu	A	1.5	16	13	13	19	20	24	22	13	211	A	25	3	-
5	196Y5A0504	BODDUNA CHANDANA	1	2	3	A	·u	5	6		2		0	A	11	12	13	111	10	16	17	18	A	19	20	21	72	73	20	25	26	2
6	196Y5A0505	CHINDAM AKANKSHA	1	2	3	u	5	6	7		8		10	11	12	13	4	15	14	A	17	13			21	22	23	24	25	26	27	
7	196Y5A0506	MUSUKU PRAVALIKA	7	2	3	A	4	5	6		-	_		A	it	12	13	14	15	16	A	17	18		20		22			24	25	: :
8	196Y1A05B6	VENNAMANENI DEEPIKA	1	2	3	4	S	6	D	7 .	8 0		0	11	12.	13	A	(4	15	16	17	18	19	A	20	2)	22	23	20	25	26	-
9	196Y1A05B7	YADA SRIVALLI	1	2	2	4	5	6	7	0	9 1	in i	1	A	12	13	u	15	16	17	18	19	20	21	22	23	211	25	26	22	25	3 2
10	196Y1A05B8	YERRABELLI SRINITHYA	1	2	3	4	A	5	6	7	8	9 10	0	11	12	A	13	14	15	16	A	17	18	19	20	21	22	A	72	21	1 25	
11	196Y1A05B9	POGULA INDU	1	2	3	.4	5	6	7	A	8 0	9 1	0	11	12.	13	14	15	A	16	17	18	19	20	21	77	23	20	25	26	27	
12	206Y5A0501	AKULA CHANDANA	1	2	3	a	4	5	6	7	8	- 1	10	A	11 1	2	13	14	15	16	А	12	18	19	20	21	27	77	20	25	26	
13	206Y5A0502	KOTA SAI KASTURI	1	2.	3	u	5	6	7			10	A-	11	12	13	14	15	16	17	12	.19	20	21	22	23	24	25	26	A	27	+
14	206Y5A0503	LAKKA PRIYA	1	2	3	ч	5	6	A	2	8 1	9/1	01	u	12	13	14	A	15	16	17	13	19	20	21	22	23	20	25	26	27	_
15	206Y5A0504	MANDA SAI ANJANI	1	2	3	u	5	6	7	8	9-11	0 1		0	12	13	A	14	15	6	17	18	19	20	24	22	23	24	25	26	27	
16	206Y5A0505	MOHAMMAD SHABANA ANJUM	1	2	3	ч	5	6	7	8	AC	7 10	0 1	ll	12	13	A	14		16	17	A	18	19	20	21	22	23	A	24	25	_
17	206Y5A0506	PALIKA DIVYA DARSHINI	1	2	3	u	A	5	6	7 8	3 <	1 1	0	ii	A	12 1	3	14	1.5	16	17-	12	19	A	20	21	22	23	24	25	26	2
18	206Y5A0507	PANGA PAVANI	1	2	A	3	4	S	6	7 3	8 0	9 1	0	١	12	13	14	15	16	4	12	19	20	21	22	13	24	A	25	26	_	1
19	206Y5A0508	PASUNURI ESTHERA	1	2	3	u	A	5	6	7	8 0	9/1	0	h	121	3	A	14	15	16	17	18	19	A	20	21	22	23	24		26	-
20	206Y5A0509	SIRIMALL TRIVENI	1	2.	3	4	5	6	4	8	2 1	0 1	11	12	13 1	4	15	16	17	18	19	20	21	22	23	24	25	_	27	- 28		
21	206Y5A0510	VEMURI AKSHITHA	1	2	A	3	3	5	6	7 5	3 (	96	A	10	it !	12.	13	14	15	16	17	18	19	20		22	A	23	24	25		2
22	206Y1A0412	BOPPA AKHILA	1	2	3	4	A	.5	6	7	8 0	7	10	11	12	13	14	15	A	16	17	18	19	20	A	21	22	23	24		26	2
23	206Y1A0413	BUDDHE SANGEETHA	1	2	3	a	5	6	Q	7	3 (	2 11	01	1	12	AI	3	14	15	16	17	28	19	20	21	A	22	72	A	24	25	
24	206Y1A0414	BURLA HARIKA	1	2	A	3	4	5	6	7	8	9/11	0 1	11	12	13	A	14	15	16	17	A	18	19	20		22		24	20	26	2
25	206Y1A0415	CHERUKUPALLY KEERTHANA	1	2	3	4	5	6	7	8	a	ali	01	i	12	13	14	A	15	10	17	18	19	20	A	21	A	22	23	24	25	2
26	206Y1A0416	CHINTHAREDDY DIVYASRI	1	2	3	u	5	A	6	7	80	7 1	A	10	A	11	12	13	14	15	6	17	18	19	20	21	A	22	23	24	25	2
27	206Y1A0417	DEVATHI MADHUMITHA	1	2	3	4	5	6	7	8	2 1	01	1 1	12	A	13	14	15	16	17	13	9	20	A	21	7/2	Ai	23	24	A	25	24
28	206Y1A0418	EMMADI SATHWIKA	1	2	3	4	A	5	6	7 5	8 (	A	91	0	1	12	13	24	15	16	A	17	18	19	20	AK	2	22	23	24	25	2
29	206Y1A0419	ENUGALA SOUJANYA	1	2	A	3	u	5	A	76	7	8 1	7	9	0	A	Ú.	12	131	4	18	16	17	17	19	20	21	22	23	24	25	2
30	206Y1A0420	GORANTALA HARSHITHA	1	A	2	3	u	5	6	7	8	91	10	11	12	13	14	A	15	16	17	Ã	18	19	11.0	20	Li.	CH	19	_		2
31	206Y1A0421	GOURI PRIYA YAMSANI	1	2	A	3	ч	5	6	7	8	AC	7	10	11	12	A	13	14	15	A	Bu	math	IN Re	didy	Insti	tuto	ODE	dhn	oteg	v toc	W
32	206Y1A0422	GUMMADAVELLI DEEKSHITHA	1	2	3	U	5	6	7		a	10	11	12	131	41	S		17		13	n	20	34	32	33	24	20	36	3	PR	Â
33	206Y1A0423	HATKAR DEEPIKA	1	2-	3	4	5	6	7	8	A	9/1	01	1	12	131	10000	15	10			19	20	24	22	72	24	An	25	26	23	2
34	206Y1A0424	HUZAIFA GAZNAM	1	1	A	3	u	5	6	7	80	91	0	11	470	The same of the	13	14	15	A	16	17	18	19	20	IA	24	26 20 22	23	24	A	2
35	206Y   A0425	JAKKULA VAISHNAVI	1	2	3	u	5	6	7	80		1101	1	12	13 1	4	15	10	17	A	18	19	20	24	22	A	72	24	A	25	26	5
36	206Y1A0426	JANAGANI BHAVANA	1	A	2	3	4	5	6	2	0	91	0	11	12	13	A	14	15	14	19	13	10	A	20			22				1

Academic year 2019-20

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1	186Y1A05B7	VIJAYAGIRI SAI NIKITHA	28	20	A	30	31		88	113		nis)					71							WIT								
2	196Y5A0501	ALIYA MEHREEN	_	28	29				88	11 18					14		1	100	10.1			100							1			1
3	196Y5A0502	AYESHA SULTHANA	30	31			34		97					17.0	1 4			58								1 2						
4	196Y5A0503	BALASANI VENNELA	28	29	30	119 10	32		91					110	77						1											
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7	196Y5A0506	MUSUKU PRAVALIKA	27	28		-	31		88						h	34													TIE.			
8	196Y1A05B6	VENNAMANENI DEEPIKA	28	29		_	32		91		1											12=										
9	196Y1A05B7	YADA SRIVALLI	30		32	110.11	24		97	N. S												- 3			1	13:1		111				
10	196Y1A05B8	YERRABELLI SRINITHYA	27			30			88			14									- 71											
11	196Y1A05B9	POGULA INDU	29	1000	31	115-2	A		94																							
12	206Y5A0501	AKULA CHANDANA	28					15	88		1								10													
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14	206Y5A0503	LAKKA PRIYA	29	10.00	31	-																										
15	206Y5A0504	MANDA SAI ANJANI	29	10000	31	31197	CONTRACT OF STREET		94	4116																						
16	206Y5A0505	MOHAMMAD SHABANA ANJUM			20	207	0		88	1																		7.7				D/I
17	206Y5A0506	PALIKA DIVYA DARSHINI	28		30	(Partition)	111111111111111111111111111111111111111		91																						4	
18	206Y5A0507	PANGA PAVANI	20		31				94																						GE T	
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20	206Y5A0509	SIRIMALL TRIVENI	31	32			-		100					r i		-													11.0			-
21	206Y5A0510	VEMURI AKSHITHA			30	.31	32	4	91																							
22	206Y1A0412	BOPPA AKHILA	28	29	30	31	32		91													9										
23	206Y1A0413	BUDDHE SANGEETHA	27	27	20				88							Ti				43												
24	206Y1A0414	BURLA HARIKA	28	20	.30	-			91								74															П
25	206Y1A0415	CHERUKUPALLY KEERTHANA	27		29				88																				18			
26	206Y1A0416	CHINTHAREDDY DIVYASRI	2	+28			Process of the last		88		8.1	l D														RF.						
27	206Y1A0417	DEVATHI MADHUMITHA	27			The state of			88													1				0	1					
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29	206Y1A0419	ENUGALA SOUJANYA	2-1		29				88						F												-		-			
30	206Y1A0420	GORANTALA HARSHITHA	1000 1007	100000000000000000000000000000000000000	28	15 BY 20 CM	100000000000000000000000000000000000000		85								1				7					Pri	no	ip	al			
31	206Y1A0421	GOURI PRIYA YAMSANI			29				88													Sun	athi	Rec	dy l	nstitu	rte o	Ter	hno	ogv I	or W	om
32	206Y1A0422	GUMMADAVELLI DEEKSHITHA	30	31	32	33	24		97	1													100	nth.	100	125	ΛΛ	Ha	200	37	24	141
33	206Y1A0423	HATKAR DEEPIKA			31				94				-									-	uld	ALA	DOC	Jai		500	27	C	hy () S)	<del>n)</del>
34	206Y1A0424	HUZAIFA GAZNAM	26		28				85														- 1	NA	W	IG/	r-	200	3/	111	9)	-44
35	206Y1A0425	JAKKULA VAISHNAVI		20	30	31	32		91	10			,											,								
36	206Y1A0426	JANAGANI BHAVANA	22	28	201	30	21		88																							Tah (s

Academic year 2019-20

	EMBEDD	DED SYSTEMS								BAT	CH-	2 .	7/4/1							(	Cour	se In	struc	ctor:	K.K	OTI	ESHV	VAR	RAC	С		
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SNO	ROLL NO	NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
37	206Y1A0427	JANGALA LAXMI PAVANI	1	2	3	4	5	6	7	A	9	10	11	12	13	14	1.5	16	17	18	A	19	20	4	22	A	23	24	25	26	27	28
38	206Y1A0428	JERIPOTHULA CHANDANA	1	A	2	3	4	5	6	7	8	9	10	A	11	12	13	14	13		17	18	19	A	20	_	22	-	24	1000		27
39	206Y1A0429	KADIVENDI POOJITHA	1	2	3	u	5	6	A	4	8	q	O	17	12	13	A	lu	15	16	17	18	19	20	21	22		24	1000	A	206	77
40	206Y1A0430	KALERU SAI SRUTHI	1	2	3	u	5	6	7	8	9	10	A	U	12	13	14	15	16	17	18	72727	20	21	22	23		25	26	27	25	25
41	206Y1A0431	KOTHAKONDA HARIKA	1	2	3	4	A	5	6	7	8	a	10	11	12	13	14	T	16	17	18	4	120	20	1227		22			25	A	26
42	206Y1A0432	KUCHANA AMULYA	4	2	3	ч	.5	A	6	4	8	a	A	10	11	12	1.3	14	15	16	17	12		20			23			A	26	27
43	206Y1A0433	MADASU MADHU SREE	1	2	A	3	4	5	6	7	2	A	Q	10	11	17	12	14	15	16	17		10	10000	The second		1000			25	100000000000000000000000000000000000000	27
44	206Y1A0434	MANDA AISHWARYA	A	1	2	3	4	.5	6	7	8	a	10	11	A	12	13	ly	15	16	10	A	18	10	20	A	21	27	73	24		26
45	206Y1A0435	MANDA KEERTHANA	1	2	3	4	5	6	7	A	8	a	10	11	12	A	13	14	15	16	A	12	19	20	21	A	22	23	24	-	26	27
46	206Y1A0723	YERRA SAISREE	1	21	3	u	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	A		22	-23	24			79		28

Rijan

Principal
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ACADEMIC YEAR 2019-20

1	EMBEDDED SYSTEMS
	DATE:

NAME

JANGALA LAXMI PAVANI

JERIPOTHULA CHANDANA

KADIVENDI POOJITHA

KOTHAKONDA HARIKA

MADASU MADHU SREE

MANDA AISHWARYA

MANDA KEERTHANA

YERRA SAISREE

KALERU SAI SRUTHI

KUCHANA AMULYA

ROLL NO

206Y1A0427

206Y1A0428

206Y1A0429

206Y1A0430

206Y1A0431

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206Y1A0433

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Ch. Sicoly Course Co-odinator

Rijar Principal

Sumathi Reddy Institute of Technology for Women Ananthasagar (V), Hasanparthy (M) WARANGAL - 506 371 (TS)

#### Students Eligible for Certification as per Eligibility Criteria

Course: Embedded Systems Date: 19-10-2019 to 22-11-2019

S.No	Roll number	Name	Marks
1	166Y1A0476	VEMULA SACHIVYA REDDY	20
2	166Y1A0477	VENUVANKA MANSI	22
3	166Y1A0478	VURLUGONDA SOUMYA	19
4	166Y1A0479	ZILPELLIWAR SREEJA	18
5	16C31A04D3	SUNKISHALA RACHANA	22
6	176Y5A0401	ALAKANTI SHUSHMA	22
7	176Y5A0402	ALUGOJU SPANDANA	20
8	176Y5A0403	EJJAGIRI ANUSHA	22
9	176Y5A0404	GORAD ASHWINI	19
10	176Y5A0405	MANTHRI SHASHIKALA	18
11	176Y5A0406	MODEM DIVYA	22
12	176Y5A0407	PABBU ANUSHA	22
13	176Y5A0408	SAMALA VYSHALI	20
14	176Y5A0409	SOORA SAI LAXMI	22
15	186Y5A0401	ADEPU DEEKSHA	19
16	186Y5A0402	ADEPU DEVIKA	18
17	206Y1A0432	KUCHANA AMULYA	22
18	186Y5A0404	CHALLA AKHILA	22
19	186Y5A0405	GANDRA SOUMYA	20
20	186Y5A0406	GUDIKANDULA PREETHI	22
21	186Y5A0407	JANGAM RASHMA	19
22	186Y5A0408	KADARI NETHRA	18
23	186Y5A0409	KATKURI DEEPIKA	22
24	186Y5A0410	KONDABOINA VENNELA	22
25	186Y5A0411	KOTHA PRANAYA	20
26	186Y5A0412	KOTHAKONDA PRIYADARSHINI	22
27	186Y5A0413	PINNINTI HIMABINDU	19
28	186Y5A0414	PONNAM GOUTHAMI	18
29	186Y5A0415	RANGU PRIYANKA	22
30	186Y1A05B2	TULA AKANKSHA	22
31	186Y1A05B3	UDUTHA DIVYA	20
32	186Y1A05B4	UTNOORI NITHYA SRI	22
33	186Y1A05B5	VEDA SRESHTA MADAVA PEDDI	19
34	186Y1A05B6	VENGALA VYSHNAVI	18
35	186Y1A05B7	VIJAYAGIRI SAI NIKITHA	22
36	196Y5A0501	ALIYA MEHREEN	22
37	196Y5A0502	AYESHA SULTHANA	20

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38	196Y5A0503	BALASANI VENNELA	22
39	196Y5A0504	BODDUNA CHANDANA	19
40	196Y5A0505	CHINDAM AKANKSHA	18
41	196Y5A0506	MUSUKU PRAVALIKA	22
42	196Y1A05B6	VENNAMANENI DEEPIKA	22
43	196Y1A05B7	YADA SRIVALLI	20
44	196Y1A05B8	YERRABELLI SRINITHYA	22
45	196Y1A05B9	POGULA INDU	19
46	206Y5A0501	AKULA CHANDANA	18
47	206Y5A0502	KOTA SAI KASTURI	22
48	206Y5A0503	LAKKA PRIYA	22
49	206Y5A0504	MANDA SAI ANJANI	20
50	206Y5A0505	MOHAMMAD SHABANA ANJUM	22
51	206Y5A0506	PALIKA DIVYA DARSHINI	19
52	206Y5A0507	PANGA PAVANI	18
53	206Y5A0508	PASUNURI ESTHERA	22
54	206Y5A0509	SIRIMALL TRIVENI	22
55	206Y5A0510	VEMURI AKSHITHA	20
56	206Y1A0412	BOPPA AKHILA	22
57	206Y1A0413	BUDDHE SANGEETHA	19
58	206Y1A0414	BURLA HARIKA	18
59	206Y1A0415	CHERUKUPALLY KEERTHANA	22
60	206Y1A0416	CHINTHAREDDY DIVYASRI	- 22
61	206Y1A0417	DEVATHI MADHUMITHA	20
62	206Y1A0418	EMMADI SATHWIKA	22
63	206Y1A0419	ENUGALA SOUJANYA	19
64	206Y1A0420	GORANTALA HARSHITHA	18
65	206Y1A0421	GOURI PRIYA YAMSANI	22
66	206Y1A0422	GUMMADAVELLI DEEKSHITHA	22
67	206Y1A0423	HATKAR DEEPIKA	20
68	206Y1A0424	HUZAIFA GAZNAM	22
69	206Y1A0425	JAKKULA VAISHNAVI	19
70	206Y1A0426	JANAGANI BHAVANA	18
71	206Y1A0427	JANGALA LAXMI PAVANI	22
72	206Y1A0428	JERIPOTHULA CHANDANA	22
73	206Y1A0429	KADIVENDI POOJITHA	20
74	206Y1A0430	KALERU SAI SRUTHI	22
75	206Y1A0431	KOTHAKONDA HARIKA	19

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166y1A0U77 V. Mani Test(Embedded Systems)
Duration: 1hr  1. Which design allows the reuse of the software and the hardware components?  a) Memory Design b) Input design c) Platform-based design d) Peripheral design
2) Which design considers both the hardware and software during the embedded design?( b) a) Memory Design b) Software/ hardware co design c) Platform-based design d) Peripheral design
3) What does API stand for? a) Application Programming Interface c) Accessing peripheral through the interface d) none of them
4) Which process can be used in analyzing the set of possible designs? a) Scheduling b) Design space exploration c) Hardware / Software partitioning d) Compilation
5) Which of the following can reduce the loop overhead and thus increase the speed? (C) ?  a) Loop tiling b) Loop unrolling c) loop fusion d) loop permutation
6) Which part of the COOL input comprises information about the available hardware platform components? a) Design constraints b) target technology c) Behavior d) both behavior and design constraints
7) What does Index set L denotes? a) Task graph node b) processor c) Hardware components d) task graph node type
8) Which design can be used to reduce the energy consumption of the embedded system? (b) a) Simulator b) Compiler c) Emulator d) Debugger
9) Which model is based on precise measurements using real hardware? a) First power model b) Encc energy-aware compiler c) Second Power Model d) Third power model
10) Which of the following function can interpret data in the C language?  a) Scanf  b) Printf  c) File  d) Proc  l) Which of the following function can interpret data in the C language?  (A)
11) Which statement replaces all occurrences of the identifier with string?  a) # include b) # define identifier string b) c) # ifdef d) # define MACRO()  12) Which command takes the object file and searches library files to find the rotatile cans.

a) Emulator b) Simulator c) Linker d) Debugger

Principal

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Ananthasagar (V), Hasanparthy (M)

WARANGAL - 506 371 (TS)



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5) Which model is used to denote the Boolean functions? (a) Simulator (b) Strength (c) Layout model (d) circuit Prancipal	
) Algorithmic Level d) Switch Level	
4) Which level simulates the algorithms that are used within the embedded systems? (C)  (Circuit Level b) Gate Level	
23) Which of the following is an analog extension of the VHDL?  (b) System VHDL b) VHDL-AMS c) System Verilog d) Verilog	
(22) Which C++ class is similar to the hardware description language like VHDL? ( g) Verilog b) C c) JAVA d) SystemC	
21) How can one compute the power consumption of the cache?  a) First power model b) Lee power model c) CACTI d) Third power model	
20) Which of the given networks are based on the compensation theorem?  a) Unilateral network  b) Bilateral network  c) Linear and non-linear network  d) Distributed network	
19) Which models communicate between the components?  a) Fine-grained modeling b) transaction level modeling c) circuit-level model d) coarse-grained modeling	
18) Which of the following is an abstraction of the signal impedance? a) Strength b) Nature c) Size d) Level	
17) Under no-load conditions, the transmission line carrying a current because  a) Heating effect  b) Capacitance effect  c) Chemical effect  d) Transmission effect	
16) Which of the following can compute the exact number of clock cycles require to run application?  a)coarse-grained model b)layout model c) register-transaction model d) fine-grained model	
a) gate-level model b) switch level c) layout model d) circuit level	
a) C b) JAVA C) System C d) C++	3
13) What describes the connections between the entity port and the local component? (d) a)One-to-one map b) Many-to-one map c) One-to-many maps d) Port map	



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#### Paiyanka Test(Embedded Systems)

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1. Which design allows the reuse of the software and the hardware components?

a) Memory Design

b) Input design

c) Platform-based design

d) Peripheral design

2) Which design considers both the hardware and software during the embedded design? (b

a) Memory Design

b) Software/ hardware co design

c) Platform-based design

d) Peripheral design

3) What does API stand for?

a) Application Programming Interface

b) Address Programming Interface

c) Accessing peripheral through the interface

d) none of them

4) Which process can be used in analyzing the set of possible designs?

a) Scheduling

b) Design space exploration

c) Hardware / Software partitioning

d) Compilation

5) Which of the following can reduce the loop overhead and thus increase the speed? (-b)

a) Loop tiling b) Loop unrolling c) loop fusion d) loop permutation

6) Which part of the COOL input comprises information about the available hardware platform components?

a) Design constraints

b) target technology

c) Behavior

d) both behavior and design constraints

7) What does Index set L denotes?

a) Task graph node

b) processor

c) Hardware components

d) task graph node type

8) Which design can be used to reduce the energy consumption of the embedded system? (

a) Simulator b) Compiler c) Emulator d) Debugger

9) Which model is based on precise measurements using real hardware?

a) First power model

b) Encc energy-aware compiler

c) Second Power Model

d) Third power model

10) Which of the following function can interpret data in the C language?

a)Scanf

b) Printf

c) File

d) Proc

11) Which statement replaces all occurrences of the identifier with string?

a) # include

b) # define identifier string

b) c) # ifdef

d) # define MACRO()

12) Which command takes the object file and searches library files to find the router

a) Emulator b) Simulator

c) Linker

d) Debugger

Principal

(d)

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13) What describes the connections between the entity port and the local component? (da)One-to-one map b) Many-to-one map c) One-to-many maps d) Port map
a) C b) JAVA C) System C d) C++
a) gate-level model b) switch level c) layout model d) circuit level
16) Which of the following can compute the exact number of clock cycles require to run application? a)coarse-grained model b)layout model c) register-transaction model d) fine-grained model
a) Heating effect b) Capacitance effect c) Chemical effect d) Transmission effect
18) Which of the following is an abstraction of the signal impedance? a) Strength b) Nature c) Size d) Level
19) Which models communicate between the components?  a) Fine-grained modeling b) transaction level modeling c) circuit-level model d) coarse-grained modeling
20) Which of the given networks are based on the compensation theorem?  a) Unilateral network  b) Bilateral network  c) Linear and non-linear network  d) Distributed network
21) How can one compute the power consumption of the cache?  (b)  (c)  (c)  (d)  (d)
22) Which C++ class is similar to the hardware description language like VHDL? ()  a) Verilog b) C c) JAVA d) SystemC
23) Which of the following is an analog extension of the VHDL?  (b) System VHDL (b) VHDL-AMS (c) System Verilog (d) Verilog
24) Which level simulates the algorithms that are used within the embedded systems? (C)  b) Gate Level c) Algorithmic Level d) Switch Level
25) Which model is used to denote the Boolean functions?  (b) Simulator  (c) Layout model  (d) circuit Refuseing
Simulator b) Strength c) Layout model d) circuit Principal  Sumathi Reddy Institute of Technology for Women

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This is to certify that VURLUGONDA SOUMYA bearing roll number 166Y1A0478 has completed the course on "Embedded Systems" conducted from 19-10-2019 to 22-11-2019.

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Mr.Ch.Siddhardha

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Dr.K.Mahender sharma

Head of the Department

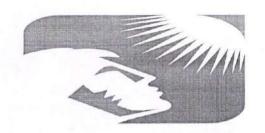
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Dr.I.Rajasri Reddy

Principal

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